In the Claims:

Claim 1 (currently amended): A sensing circuit for a target memory cell, said sensing circuit comprising:

said target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation;

a first transistor being connected to said first node;

a decouple circuit being connected to said first transistor, said decouple circuit including a second transistor having a gate width greater than a gate width of said first transistor, a gate of said second transistor being coupled to a gate of said first transistor, said decouple circuit further having a decouple coefficient (N) greater than 1, a drain of said second transistor being connected at a second node to a reference voltage through a bias resistor, said drain of said second transistor generating a sense amp input voltage at said second node such that said sense amp input voltage is decoupled from said first node.

Claim 2 (original): The sensing circuit of claim 1 wherein said gate of said second transistor is N times wider than said gate of said first transistor.

Claim 3 (currently amended): The sensing circuit of claim 1 wherein said decouple circuit [[230]] draws a mirror current N times larger than said target memory cell current.

Claim 4 (original): The sensing circuit of claim 1 wherein said first transistor comprises a first PFET, and said second transistor comprises a second PFET, said gate of said first PFET connected to a drain of said first PFET, a source of said first PFET and a source of said second PFET being connected to a supply voltage.

Claim 5 (original): The sensing circuit of claim 1 wherein said reference voltage is ground.

Claim 6 (original): The sensing circuit of claim 1 wherein said target memory cell is capable of storing four charge levels.

Claim 7 (original): The sensing circuit of claim 6 wherein said four charge levels comprises a first charge level drawing approximately 0 microamperes during said read operation, a second charge level drawing approximately 10 microamperes during said read operation, a third charge level drawing approximately 15 microamperes during said read operation, and a fourth charge level drawing approximately 20 microamperes during said read operation.

Claim 8 (currently amended): A multi-level charge memory device comprising:

a target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation; and

a sensing circuit comprising a first transistor connected to a decouple circuit, said first transistor being connected to said first node, said decouple circuit including a second transistor having a gate width greater than a gate width of said first transistor, a gate of said second transistor being coupled to a gate of said first transistor, said decouple circuit further having a decouple coefficient (N) greater than 1, a drain of said second transistor being connected at a second node to a reference voltage through a bias resistor, said drain of said second transistor generating a sense amp input voltage at said second node such that said sense amp input voltage is decoupled from said first node.

Claim 9 (original): The multi-level charge memory device of claim 8 wherein said gate of said second transistor is N times wider than said gate of said first transistor.

Claim 10 (currently amended): The multi-level charge memory device of claim 8 wherein said decouple circuit [[230]] draws a mirror current N times larger than said target memory cell current.

Claim 11 (original): The multi-level charge memory device of claim 8 wherein said first transistor comprises a first PFET, and said second transistor comprises a second PFET, said gate of said first PFET connected to a drain of said first PFET, a source of said first PFET and a source of said second PFET being connected to a supply voltage.

Claim 12 (original): The multi-level charge memory device of claim 8 wherein said reference voltage is ground.

Claim 13 (original): The multi-level charge memory device of claim 8 wherein said target memory cell is capable of storing four charge levels.

Claim 14 (original): The multi-level charge memory device of claim 13 wherein said four charge levels comprises a first charge level drawing approximately 0 microamperes during said read operation, a second charge level drawing approximately 10 microamperes during said read operation, a third charge level drawing approximately 15 microamperes during said read operation, and a fourth charge level drawing approximately 20 microamperes during said read operation.

Claim 15 (currently amended): A sensing circuit for a target memory cell, said target memory cell having a drain capable of being connected to a first node through a selection circuit during a read operation involving said target memory cell, said target memory cell drawing a target memory cell current when activated during said read operation, a first transistor being connected to said first node, said sensing circuit being characterized by:

a decouple circuit being connected to said first transistor, said decouple circuit including a second transistor having a gate width greater than a gate width of said first transistor, a gate of said second transistor being coupled to a gate of said first transistor, said decouple circuit further having a decouple coefficient (N) greater than 1, a drain of said second transistor being connected at a second node to a reference voltage through a bias resistor, said drain of said second transistor generating a sense amp input voltage at said second node such that said sense amp input voltage is decoupled from said first node.

Claim 16 (original): The sensing circuit of claim 15 wherein said gate of said second transistor is N times wider than said gate of said first transistor.

Claim 17 (currently amended): The sensing circuit of claim 15 wherein said decouple circuit [[230]] draws a mirror current N times larger than said target memory cell current.

Claim 18 (original): The sensing circuit of claim 15 wherein said first transistor comprises a first PFET, and said second transistor comprises a second PFET, said gate of said first PFET connected to a drain of said first PFET, a source of said first PFET and a source of said second PFET being connected to a supply voltage.

Claim 19 (original): The sensing circuit of claim 15 wherein said reference voltage is ground.

Claim 20 (original): The sensing circuit of claim 15 wherein said target memory cell is capable of storing four charge levels.